IN THE CLAIMS:

Claims 1-17, 25-32, and 40-47 were previously cancelled. Claim 20 has been amended herein. All of the pending claims are presented below. This listing of claims will replace all prior versions and listings of claims in the application. Please enter these claims as amended.

Listing of Claims:

1.-17. (Cancelled)

18. (Previously amended) A method of forming an electrical structure on a substrate, the method comprising:

performing a first plasma doping (PLAD) operation to form a first doped region in a substrate; and

performing a second doping operation, the second doping operation comprising depositing dopants in the first doped region and in a second doped region that is contiguous with and extends below the first doped region, wherein the first doped region has a higher dopant concentration than the second doped region, the second doped region having a lower periphery that is substantially planar and substantially parallel to a top surface of the substrate.

19. (Previously amended) The method as defined in claim 18, wherein performing a first PLAD operation to form a first doped region in a substrate comprises performing the first PLAD operation to form the first doped region having a dopant concentration that terminates relatively abruptly at an uneven lower periphery.

20. (Currently amended) The method as defined in claim 18, wherein:

performing a first PLAD operation to form a first doped region in a substrate comprises forming the first doped region having a lower periphery at a depth of less than about 1000 Å; and

performing a second doping operation comprises forming the second doped region having a lower periphery at a depth that is less than about 1750 Å from ~~a top~~ the top surface of the substrate and at least about 250 Å greater than the depth of the lower periphery of the first doped region.

21. (Previously amended) The method as defined in claim 18, further comprising annealing the substrate after at least one of the second doping operation and the first PLAD operation to cause a more uniform distribution of dopants.

22. (Previously amended) The method as defined in claim 21, wherein annealing the substrate comprises rapid thermal annealing of the substrate.

23. (Previously amended) The method as defined in claim 18, wherein:

performing a first PLAD operation to form a first doped region in a substrate comprises conducting the first PLAD operation at an energy in a range of from about 5 KeV to about 15 KeV such that the first doped region has a dopant concentration in a range of from about 1×10^{19} dopant atoms/cm^3 to about 5×10^{21} dopant atoms/cm^3; and

performing a second doping operation comprises performing the second doping operation at an energy in a range of from about 10 KeV to about 25 KeV such that the second doped region has a dopant concentration in a range of from about 1×10^{16} dopant atoms/cm^3 to about 1×10^{19} dopant atoms/cm^3, the second doping operation being conducted in a medium power implanter operating in a range of from about 0 KeV to about 200 KeV.

24. (Previously amended) The method as defined in claim 18, further comprising forming a portion of an electrical device that is selected from the group consisting of a diode, a resistor, and a transistor with the first doped region and the second doped region.

25.-32. (Cancelled)

33. (Previously presented) A method of forming an electrical structure on a substrate, the method comprising:

providing a gate region over a substrate, the gate region having a bottom surface;

performing a first plasma doping (PLAD) operation to form a first doped region in the substrate, wherein the first doped region does not underlap the bottom surface of the gate region; and

performing a second doping operation, the second doping operation comprising depositing dopants in the first doped region and in a second doped region that is contiguous with and extends below the first doped region, wherein the first doped region has a higher dopant concentration than the second doped region, the second doped region having at least a portion thereof that underlaps the bottom surface of the gate region.

34. (Previously amended) The method as defined in claim 33, wherein performing a first PLAD operation to form a first doped region in the substrate comprises forming the first doped region having a dopant concentration that terminates relatively abruptly at an uneven lower periphery.

35. (Previously amended) The method as defined in claim 33, wherein:

performing a first PLAD operation to form a first doped region in the substrate comprises forming the first doped region having a lower periphery at a depth of less than about 1000 Å; and

performing a second doping operation comprises forming the second doped region having a lower periphery at a depth that is less than about 1750 Å from a top surface of the substrate and at least about 250 Å greater than the depth of the lower periphery of the first doped region.

36. (Previously amended) The method as defined in claim 33, further comprising annealing the substrate after at least one of the second doping operation and the first PLAD operation to cause a more uniform distribution of dopant.

37. (Previously amended) The method as defined in claim 36, wherein annealing the substrate comprises performing the annealing as a rapid thermal anneal.

38. (Previously amended) The method as defined in claim 33, wherein:

performing a first PLAD operation to form a first doped region in the substrate comprises conducting the first PLAD operation at an energy in a range of from about 5 KeV to about 15 KeV such that the first doped region has a dopant concentration in a range of from about 1×10^{19} dopant atoms/cm^3 to about 5×10^{21} dopant atoms/cm^3; and

performing a second doping operation comprises performing the second doping operation at an energy in a range of from about 10 KeV to about 25 KeV such that the second doped region has a dopant concentration in a range of from about 1×10^{16} dopant atoms/cm^3 to about 1×10^{19} dopant atoms/cm^3, the second doping operation being conducted in a medium power implanter operating in a range from about 0 KeV to about 200 KeV.

39. (Previously amended) The method as defined in claim 33, further comprising forming a portion of an electrical device that is a transistor from the first doped region and the second doped region.

40.-47. (Cancelled)